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10/023,849	12/21/2001	Atsushi Yagishita	04329.1949-01000	4501
22852	7590	02/03/2006	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			ROSE, KIESHA L	
			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.



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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/023,849
Filing Date: December 21, 2001
Appellant(s): YAGISHITA ET AL.

MAILED
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GROUP 2800

David Longo
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 17 November 2005 appealing from the Office action mailed 3 June 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Art Unit: 2822

Claim 38 is rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's Prior Art (Figs. 2a/2b).

Applicant's Prior Art (Figs. 2a/2b) contain a substrate (1), a gate wiring layer (3) formed on one major surface of the substrate, an insulating film (10) interposed between substrate and gate wiring layer and covering a side surface of the gate wiring layer, a pair of thin films (5) formed on one major surface of substrate and arranged on two sides of the gate wiring layer, a gate sidewall (4) formed on pair of thin films covering side surface of gate wiring layer and made of an insulator wherein a region of pair of thin films between gate sidewall and substrate, a remaining region of pair of thin films (region under diffusion region 6 (area to the left of portion 5 in Fig. 2b)) on which gate sidewall is absent and a surface region of substrate in contact with remaining region contain a semiconductor and conductive impurity.

Allowable Subject Matter

Claim 39 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument

The appellant primarily argues one basic point; (1) that the Applicant's Prior Art (APA) (Figures 2a/2b) does not disclose a pair of thin films arranged on two sides of said gate wiring layer and a remaining region of said pair of thin films on which said gate

Art Unit: 2822

sidewall is absent. In regards to appellant's arguments, the examiner disagrees with appellant's assessment of the APA since as can be seen in Fig. 2a there are a pair of thin films (5) that are formed on the two sides of the gate wiring layer (3) and the sidewalls (4). As seen in Fig. 2b, the diffusion regions (6) are formed over the pair of thin films (5) but it does not remove the pair of thin films from the device they are just formed underneath the diffusion regions. With that said then the pair of thin films are still formed on the two sides of the gate wiring layer and the sidewalls and shows that there are remaining regions of thin film (5 formed under diffusion regions 6) which are absent from the gate sidewall, since the pair of thin film are still formed under the diffusion region (6).

In conclusion, the APA shows all the limitations of the claims including the pair of thin films arranged on two sides of the gate wiring layer and a remaining region of said pair of thin films on which gate sidewall is absent. The examiner submits that the rejection under 35 U.S.C. 102 is proper and should be affirmed.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,


Application/Control Number: 10/023,849
Art Unit: 2822

Page 6

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January 24, 2006

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2822

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2884